EXPERIMENT #7
PHASE LOCKED LOOP

INTRODUCTION:

The phase-locked loop, or PLL, is one of the most useful blocks in modern electronic circuits. It is used in many different applications, ranging from communciations (FM modulation, demodulation, frequency synthesis, signal correlation), control systems (motor control, tracking controls, etc), as well as applications such as pulse recovery and frequency multiplication. Knowing PLLs can really boost your "tech IQ!"

PLL Theory of Operation

A PLL is a closed-loop system whose purpose is to lock an oscillator onto a provided input frequency (sometimes called the *reference* frequency.) By "closed-loop," we mean that there is feedback from output to input. In a PLL, negative feedback is used, which makes it self-correcting. Figure 1 shows the block diagram of a typical PLL.

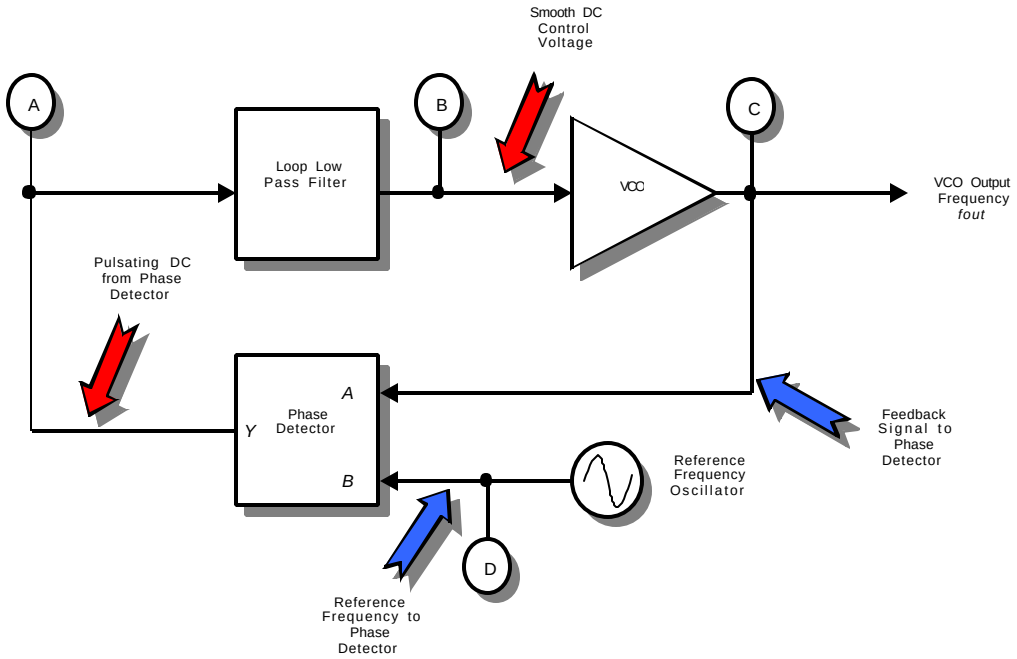

Figure 1: Phase Locked Loop Block Diagram

A PLL has a special oscillator, a VCO. We know that a VCO changes its output frequency based on input voltage (as well as R_t and C_t choices). *The primary objective of PLL operation is to get the VCO frequency to be exactly equal to that of the reference frequency*. When this happens, the loop is said to be "in lock."

This is achieved by feeding both the VCO output and the reference frequency into a *phase detector.* The phase detector compares the phase of the two waves and outputs a pulsating DC waveform with a duty cycle proportional to the phase difference (error) between the two signals. Why compare phase and not frequency? The answer is that if we compare frequency, then there will always be a small frequency error in our result. However, if we compare *phase*, the frequency error is reduced to zero whenever the phase difference is a constant.

This is easier to visualize if you think about synchronizing the speed of two cars. Two cars do not have to be in exactly the same position (phase) on the highway to have the same speed. One can be following the other at a fixed distance

(fixed phase difference). As long as they aren't speeding up or slowing down relative to each other, their speeds (frequencies) will be exactly the same.

This is why a phase detector is used instead of a "frequency detector" in a PLL. *The use of a phase detector reduces the frequency error of the closed loop system to zero.*

The output of the phase detector is a pulsating DC with a varying duty cycle. The bigger the phase difference becomes (within certain limits, of course), the larger duty cycle becomes. But the VCO needs a nice, steady DC voltage at its control voltage input. Can you imagine the effect of the pulsating DC on the VCO? Think of a car that only has two throttle positions, wide open and off. The speed limit is 55. Or was it 85? You can imagine how rough the motion of the car would be! The same thing would happen to the VCO. We'd like its output frequency to be fairly steady, like the reference input. What we need to do is smooth out the pulsating DC from the phase detector into a steady *DC average* voltage. This is the purpose of the *low-pass filter*. This filter smooths the rough phase detector output waveform into a fairly steady DC voltage for the VCO. The VCO will then be able to smoothly track the input reference frequency.

PLL Operating States

A PLL has three operating states. These are the *free-running, capture,* and *locked* conditions.

In the free-running state, there is no reference input frequency being provided to the PLL. Design constants within the system determine what frequency the VCO will run at. Normally, two of these are the values of R_t and C_t, the VCO timing components.

In the capture state, which is usually short-lived, the PLL has just been given a reference frequency, and it is in the process of trying to "lock" onto it. The PLL cannot lock onto all frequencies; only a certain range of frequencies, within the *capture range* can be locked onto, if the PLL is initially in the free-running state. The free-running frequency is usually in the middle of the capture range. The width of the capture range is determined by PLL design; the loop low-pass filter is important in determining this.

The last PLL state is the desired state: Locked! In this state, the PLL has successfully passed through the capture phase, and it has its VCO steadily "locked" onto the input reference frequency. The PLL cannot remain locked for all frequencies, and if the input reference frequency moves outside the *lock range* (which is usually larger than the capture range), the PLL will drop out of lock.

Figure 2 illustrates the relationship between free-running frequency, capture range, and lock range.

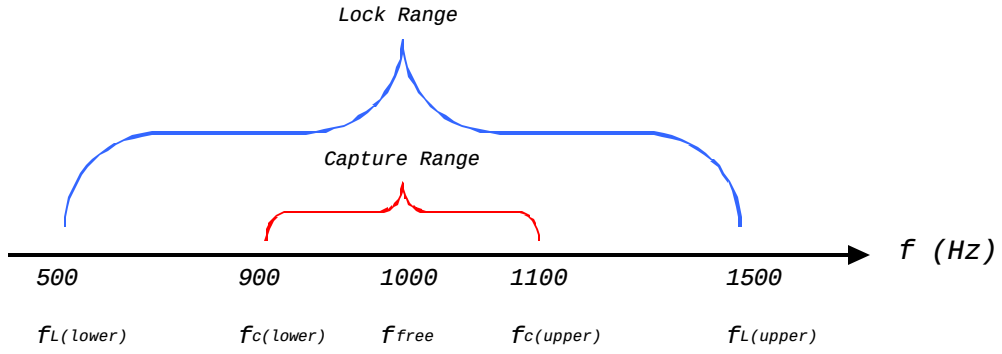

Figure 2: PLL Operating Regions

CIRCUIT ANALYSIS:

The PLL in this circuit is entirely contained within one IC chip, the LM-565.

All that we need to provide to build a complete functioning PLL are timing elements (R_t, C_t) for the VCO and a capacitor for the low-pass filter. (The LM-565 has a 3.6K resistor on-chip for the low-pass filter.)

In Figure 3 the VCO timing is set by R1, R2, and C2. The low-pass filter time-constant (which we will vary) is formed by the internal 3.6K resistor on pin 7 and C5. The reference input goes to pin 2, one of the phase detector inputs. The other phase detector input on pin 5 is directly connected to the VCO output on pin 4, closing the loop.

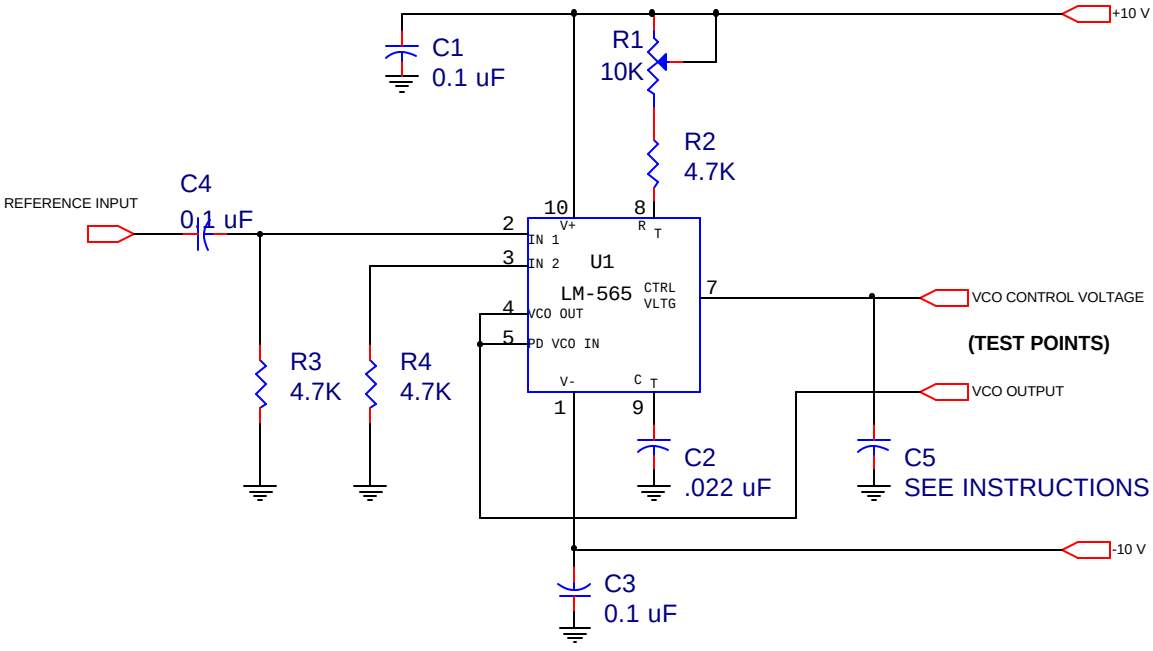

Figure 3: PLL Evaluation Circuit using the LM-565

LABORATORY PROCEDURE:

Name _____ Sign-off _____

In this experiment, you will observe the operation of the PLL subsystem. You'll learn to recognize the three PLL states in actual circuits, and you will also gain some insight into how circuit values affect PLL operation.

To get accurate frequency readings, it is strongly suggested that you use a frequency counter. Some of the frequency readings will be fairly close in value. If you have the *audio monitor* available, connect its input to the VCO OUTPUT of the PLL circuit so that you can hear the PLL going in and out of lock.

1. Construct the circuit of Figure 3 using a 10 µF electrolytic for C5. (C5 is the capacitor for the loop low-pass filter.)

2. Apply power to the circuit, but don't apply a reference signal yet. We want to set the free-running frequency of the VCO. Adjust R1 until the output frequency of the VCO on pin 4 is 1 KHz.

3. Apply the reference frequency to the *reference input* of the circuit.

4. Connect scope channel #1 to the reference input of the circuit, and scope channel #2 to the VCO output. Connect the frequency counter to the *reference input*, so that the frequency of the reference is displayed. (Be sure to trigger off channel #1, the reference input.)

5. Set the function generator to 600 Hz, 1 Vpp sine. Observe the two scope traces and describe what you see below. Does the loop appear to be in lock, or out-of-lock at this point? Why?

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6. Slowly increase the frequency of the generator until the PLL just locks. (The two traces appear stable on the scope). A phase shift will be present between the VCO and reference frequency; this is OK. This frequency is the bottom of the capture range, $F_C(lower)$, as shown in Figure 2. Record it below.

   $F_C(lower)$ = _____

   TIP: You can always tell that the PLL is truly in lock by observing that the frequencies of the reference and VCO are identical. You may observe "false locks" during this procedure; the reference and VCO frequencies will not be equal under a false lock condition!

7. When the PLL is in lock, how do the the VCO and reference input signals compare?

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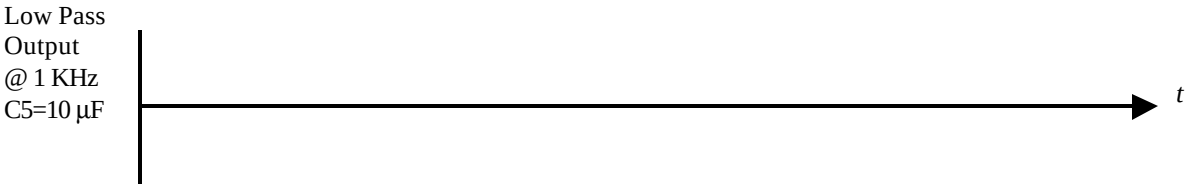
8. Let's find the top of the lock range. Slowly increase the frequency until the PLL again drops out of lock. This frequency is the top of the lock range, $F_L(upper)$. Record it below.

$F_L(upper)$ = _____

9. The PLL is now out of lock, and the reference frequency is above the top of the capture range. Slowly decrease the reference until the PLL locks again; this is $F_C(upper)$. Finally, decrease the reference frequency until the PLL drops out of lock again; this is $F_L(lower)$. Record these values.

$F_C(upper)$ = _____ $F_L(lower)$ = _____

10. Let's observe the output from the low-pass filter, to see what happens when the input frequency changes. We know it is supposed to be smooth DC, so we'll need to use the DC setting of the scope to see the DC component. We also know that no filter is perfect, so some AC ripple will be present on top of the DC. Set the reference frequency to 1 KHz, and record the low-pass filter output on pin 7 of the IC:



11. Increase the input frequency (but keep it within the lock range). What happens to the filter DC output? (You may want to measure pin 7 with a DC multimeter to get more precise voltage readings).

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12. The capture range depends on the low-pass filter of the PLL. Let's see how. Replace C5 with each value in the table below, and measure the width of the capture and lock ranges for each case.

C5 Value	F_C(lower)	F_C(upper)	F_L(lower)	F_L(upper)
10 µF				
1 µF				
0.1 µF				
0.001 µF				

13. Study the data in the above table carefully. Describe the relationship between the capture range and size of the filter capacitor in the low-pass filter according to the data in your table.

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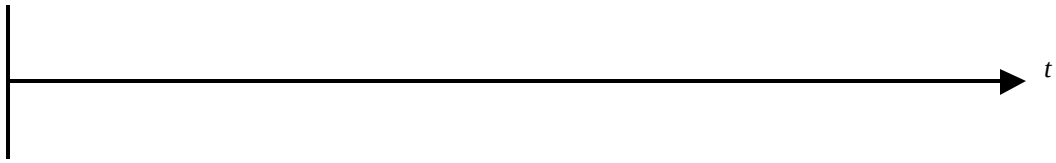
14. With the 0.001 µF capacitor in place, again set the reference frequency to 1 KHz and record the low-pass filter output. Make sure the scope is set for DC coupling.

Low Pass
Output
@ 1 KHz
C5=0.001 µF



15. How does the waveform in step 14 differ from that obtained in step 10, and why?

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16. From your data in step 12, what is your conclusion about the effect of the low-pass filter on the *lock range* of a PLL?

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QUESTIONS

1. What is the purpose of a phase locked loop?

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2. List the three main parts of a phase locked loop and briefly describe what each one does.

1) _____

2) _____

3) _____

3. List the three states of a phase locked loop.

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4. Explain how to use test equipment to determine that a PLL is in lock.

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5. What else have you learned in this experiment?

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